EXHIBIT 7

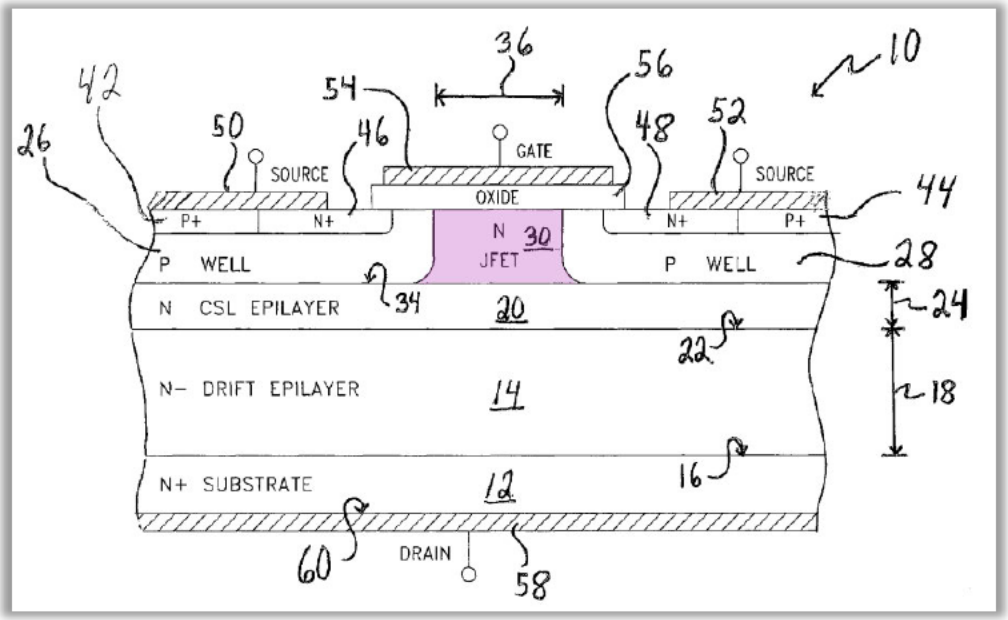
IN THE UNITED STATES DISTRICT COURT
FOR THE MIDDLE DISTRICT OF NORTH CAROLINA

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. WOLFSPEED, INC., Defendant.	CIVIL ACTION NO. 1:21-CV-840 JURY TRIAL DEMANDED

EXPERT REPORT OF STANLEY SHANFIELD, Ph.D.

CONFIDENTIAL – ATTORNEY'S EYES ONLY

42. Further, in my opinion, "the JFET region having a width less than about three micrometers," as used in the '633 Patent and in Claim 9, means exactly that. A POSITA understands the meaning of the JFET region, which is also apparent from Fig. 1 below (annotated with color for additional clarity).



See also Wolfspeed, Inc. v. The Trustees of Purdue University, No. 2022-00761, Paper 2 at 1 (similarly annotating the JFET region in pink); '633 Patent at 5:23-26 ("The semiconductor device 10 also includes two doped semiconductor wells or base regions 26, 28 formed above the current spreading layer 20 and ***a junction field-effect transistor (JFET) region 30 formed between the wells 26, 28***.") (emphasis added).

43. A POSITA would also reasonably understand the use of "about" takes into account size variations resulting from manufacturing techniques that require tolerances, or slight deviations from the ideal device design. The feature sizes prescribed in the '633 Patent are understood by a POSITA to allow for such manufacturing tolerances, or variations and such allowances do not render the claim meanings uncertain or indefinite.

44. The use of "about" is a common practice because the fabrication of SiC semiconductor devices necessarily results in minor variations in feature dimensions because of the equipment used and the microscopic feature sizes. While the average

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on "preliminary and final claim constructions." Texas Action, Dkt. 68 at 1. Dr. Yi holds a Ph.D. in electrical engineering is a POSITA. https://www.linkedin.com/in/yijoshua/details/experience/.

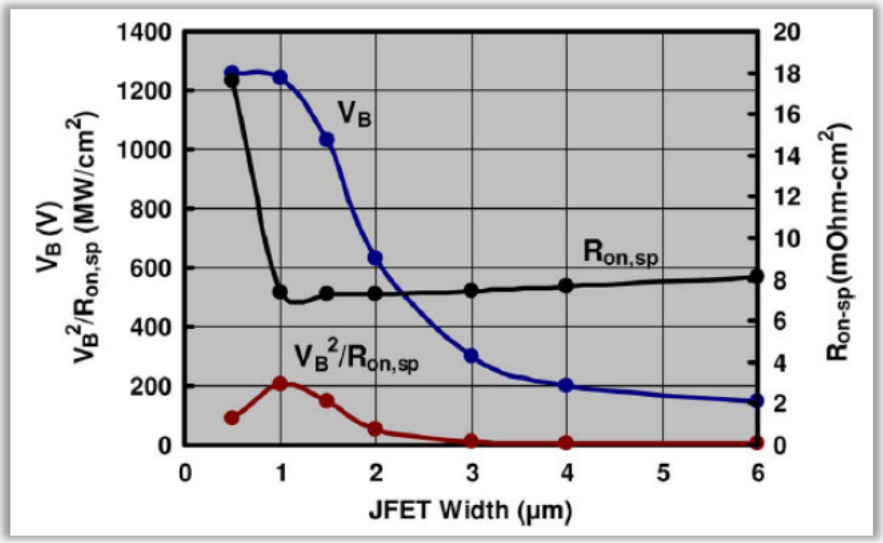
measurements of a device will be close to the specified value across the thousands of dice on a semiconductor wafer, any two devices made using the same fabrication process will have some minor deviation from this average. For example, the JFET region in the DMOSFET is fabricated by the ion-implantation process using a mask that defines the p-type base region. During the design phase, the p-well mask specifies the JFET width, which can be done precisely. However, upon fabrication, the width of the manufactured JFET depends on several factors, such as the transverse (or lateral) straggle of the ion-implantation species and species diffusion during the subsequent annealing step. Transverse straggle measures the distribution of the implanted species along the transverse direction and is dependent on many factors such as the implanting species, the host material, the implantation energy, and the final annealing temperature. Because the ion implantation process results in a distribution of the species in the vertical direction with a mean value called vertical range (R_P), and a distribution of species along the lateral direction called transverse straggle ($R_\perp$), a POSITA would know that the JFET width after fabrication cannot be specified to exact values, but rather a distribution with range and standard deviation.

45. An additional source of feature size variation is termed "CD tolerance" or critical dimension tolerance. This refers to variations in the photolithography process that defines the masking layer for the implantation. In this process, photoresist (a photosensitive film applied to the wafer) is exposed to light through a glass mask, often using a projection process. The light induces chemical changes in the photoresist layer that allow the exposed region to be chemically removed or retained, depending on the polarity of the photoresist. The process of removing a region in the photoresist involves a chemical called a developer. Because this process can either expand or contract the exposed regions of the photoresist layer, it results in an added source of variation in the feature size of implanted regions in the semiconductor.

46. Because the goal of the device design is to achieve the lowest possible on-resistance while meeting the desired blocking voltage specification ('633 Patent at 1:18-36), a POSITA would understand that a JFET region that was too wide would result in the field across the gate oxide in the blocking state to exceed the electric field for oxide breakdown, thus damaging the gate oxide. In particular, the device designer must ensure that the field in the oxide remains below a critical value to avoid early failure of the oxide during operation in the field. While most oxides will fail immediately if the field is above 9 - 10 MV/cm, in practice the oxide field must be kept below about 3 MV/cm so the device meets specifications for the intended number of years in service. On the other hand, a JFET region that was too narrow would increase the on-state resistance, contrary to the design

goal. Therefore, there is an optimum width at which one achieves the lowest on-resistance without allowing the oxide field to exceed the electric field for oxide breakdown in the blocking state.

47. A POSITA would know the design criteria of JFET-region width generally and from published literature. For example, in a 2007 paper by the inventors of the '633 Patent, the JFET-region design was attempted from 0.5 to 6 micrometers, and based on Fig. 2, shown below, it is clear to any POSITA that there is no improvement in the figure of merit for a MOSFET beyond a JFET-region width of about three micrometers. A. Saha and J. A. Cooper, "A 1-kV 4H-SiC power DMOSFET optimized for low on-resistance," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2787, Oct. 2007, attached hereto as Exhibit C.



See also Sei-Hyung Ryu, Anant K. Agarwal, Nelson S. Saks, Mrinal K. Das, Lori A. Lipkin, Ranbir Singh & John W. Palmour, "Design and Process Issues for Silicon Carbide Power DiMOSFETS," in Mat. Res. Soc. Symp. Vol. 640, pp. H4.5.1 – H.4.5.6 (2001) (evaluating 2-5 micrometer JFET width and concluding three micrometers is optimal), which is attached hereto as Exhibit D.

48. Based on the foregoing, it is my opinion that "less than about three micrometers," as used in the context of the '633 Patent, is not indefinite because a POSITA would readily understand the scope of the term with reasonable certainty.

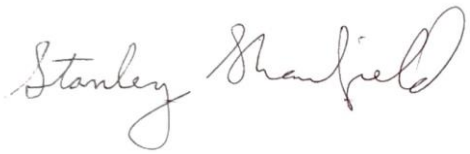
G. "the JFET region has a width of about one micrometer"

49. Consistent with my opinion above regarding "the JFET region having a width less than about three micrometers," the phrase/term "the JFET region has a width of about

one micrometer" as used in the '633 Patent and in Claim 10 is also not indefinite and needs no construction. '633 Patent at 1:65-67; 2:47-49; 3:25-26; Claim 10.

50. As explained above, a POSITA would also reasonably understand the use of the term "about" takes into account size variations resulting from manufacturing techniques that require tolerances, or slight deviations from the ideal device design. The feature sizes prescribed in the '633 Patent are understood by a POSITA to allow for such manufacturing tolerances, or variations and such allowances do not render the claim meanings uncertain or indefinite.

Dated: March 3, 2023



Stanley Shanfield